26 (amended). A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second areas are located along a side of the first semiconductor chip.

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REMARKS

The Examiner's Office Action of October 2, 2002 has been received and carefully reviewed. Claims 3-6, 8, 9, 17, 18 and 26 have been amended. No claims have been canceled. Therefore, claims 1-28 are pending in this application. For at least the following reasons, it is respectfully submitted that this application is in condition for allowance.

In the action, claims 11 and 12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification. Specifically, the examiner asserts that the non-described subject matter is the claim 11 limitation, wherein the first area is not physically connected to the first bond of the third bonding wire, and the claim 12 limitation, wherein the second area is not physically connected to the first bond of the second bonding wire. Applicant does not understand the examiner's assertion. As to claim 11, although the examiner asserts that the first area is not physically connected to the first bond of the third bonding wire, there is no such a limitation in claim 11. In claim 11, it is claimed that the first metal bump, not the first area, is not physically connected to the first bond of the third bonding wire. This claim limitation is supported by the specification on page 8, lines 7-10. As to claim 12, the same argument described above can be applied.

In the action, claims 3-12, 17, 18 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Since claims 3-6, 8, 9, 17, 18 and 26 are amended in this amendment, Applicant believes that the rejection is no longer applied to these claims. As to claim 7, 10-12, claim 7, claim 10, claim 11 and claim 12 depend from claim 6, claim 9, claim 3 and claim 4, respectively. Since claim 6, claim 9, claim 3 and claim 4 are amended in this amendment as described above, the rejection is no longer applied to these claims.

In the action, claims 13, 14, 19-23, 25, 26 and 28 are rejected under 35 U.S.C. 102(b), as being anticipated by Takiar. The inventions defined in independent claims 13, 20 and 25 relate to multi-chip package type semiconductor devices. The common characteristic of the inventions claimed in claims 13, 20 and 25 is:

(a) a first semiconductor chip having a first terminal and a conductive relay pad, the conductive relay pad including a first area and a second area (claim13),

(b) a first semiconductor chip having a first conductive portion and a second conductive portion, the second conductive portion having a first area and a second area (claim 20), or

(c) a second conductive pattern formed on the first semiconductor chip, the second conductive pattern having a first area and a second area (claim 25).

According to the characteristic (a), (b) or (c) of the invention described above, since the conductive relay pad, the second conductive portion or the second conductive portion includes a first area and a second area, the second and third bonding wires 18a 18b can be connected in the different area in them. As a result, stress of the wire

bonding on the conductive relay pad, the second conductive portion or the second conductive portion can be reduced (Refer to the specification on page 9, lines 2-4).

However, Takiar does not show or suggest above-described characteristic. That is, Takiar does **not** disclose that an electrical contact (58) includes a first area and a second area. Takiar simply discloses that an electrical contact (54) and an electrical lead (44) are connected to the electrical contact (58). Since the electrical contact (58) does not has a first area and a second area, it is not, of course, disclosed that the electrical contact (54) and the electrical lead (44) are connected to the first and the second areas of the electrical contact (58), respectively. As a result, according to Takiar, stress of wire bonding (56), (60) on the electrical contact can **not** be reduced.

Therefore, since Takiar neither show nor suggest the characteristic (a), (b) or (c) described above, each of which is defined in claims 13, 20 and 25, claims 13, 20 and 25 are deemed to be clearly patentable, and the rejection of claims 13, 20 and 25 accordingly should be withdrawn. Further, claims 14 and 19 depend from claim 13 directly, claims 21-23 depend from claim 20 directly, and claims 26 and 28 depend from claim 25 directly so the rejection of these claims also should be withdrawn.

In the action, claims 1, 2, 15 and 16 are rejected under 35 U.S.C. 102(b), as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Takiar, or further in the alternative, under 35 U.S.C. 103(a) as obvious over the combination of Takiar and Haba.

The inventions defined in independent claims 1 and 15 relate to multi-chip package type semiconductor devices. The common and specific characteristics of the inventions claimed in independent claims 1 and 15 are:

(a) the first semiconductor chip having a first terminal pad and a conductive relay pad, and the conductive relay pad including a first area and a second area (claim1),

(b) a first bonding wire connecting the first terminal pad to the first conductive pattern (claim 1 and claim 15), and

(c) the lengths of the first, second and third bonding wire are approximately the same (claim 1 and claim 15).

According to the characteristic (a) of the invention described above, stress of the wire bonding on the conductive relay pad can be reduced, as described above. Further, according to the characteristics (b) and (c) of the invention described above, it is possible to avoid unnecessary contact of the bonding wires, which are next to each other when the semiconductor device is encapsulated by a sealing material (Refer to the specification on page 8, lines 11-20).

However, neither Takiar nor Haba shows or suggests above-described characteristics. Regarding the Takiar reference, Takiar does not disclose that the first and the second areas, as explained above. Therefore, Takiar does not disclose the characteristic (a). Next, Takiar does not disclose any electrical contacts formed on a semiconductor die (22), which are connected **only** to an electrical lead (44). In other words, Takiar does not disclose any wires corresponding to the first bonding wire of the invention. Thus, Takiar does not disclose the characteristic (b). Further, Takiar discloses a fine wire conductor (60) corresponding to the second wire of the invention, and another fine wire conductor (56) corresponding to the second wire of the invention. However, Takiar does not disclose that the fine wire conductors (60) and (56) have approximately the same lengths. The examiner asserts that Takiar teaches "short wire

bond lengths." and "wire bond lengths meeting standard assembly specification". This does not mean that the fine wire conductors (60) and (56) have approximately the same lengths. This simply means that the wire length could be short, and the wire length could be determined under the standard assembly specification. Rather, it could be seen that the fine wire conductor (60) is longer than the fine wire conductor (56) in Figs 1 and 2. Moreover, as described, since Takiar does not disclose the first bonding wire, Takiar does not disclose the relationship between the first bonding wire's length and the second and the third bonding wire's lengths.

As to the Haba reference, the examiner asserts that Haba teaches wherein the length of first, second and third bonding wires 440a, 440b, 440c, respectively, are approximately the same with reference to his disclosure at column 6, lines 6-12. However, the bonding wire 440a does not correspond to the first bonding wire of the invention. The bonding wire 440a corresponds to the second bonding wire of the invention, and the bonding wire 440b corresponds to the third bonding wire of the invention. In other words, Haba does not disclose the first bonding wire of the invention. Thus, while Haba may disclose that the second and the third bonding wire have the same lengths, Haba does not disclose the relationship between the first bonding wire's length and the second and the third bonding wire's lengths. Therefore, Haba clearly does not disclose the characteristics (b) and (c). Moreover, Haba does not disclose that the first and the second areas of the conductive relay pad formed on an IC die, which is the characteristic (a). The examiner asserts that choosing the relative lengths regarding bonding wires would be a design choice. Applicant disagrees. As described above, since all lengths of the bonding wire are approximately the same, it is possible to avoid unnecessary contact of the bonding wires, which are next to each other when the

semiconductor device is encapsulated by a sealing material (Refer to the specification on page 8, lines 11-20).

Therefore, since neither Takiar nor Haba shows or suggests the characteristics (a), (b) and (c) described above, each of which is defined in claims 1 and 15, claims 1 and 15 are deemed to be clearly patentable, and the rejection of claims 1 and 15 accordingly should be withdrawn. Further, claim 2 depends from claim 1 directly, and claim 16 depends from claim 15 directly, so the rejection of these claims also should be withdrawn.

In the action, claims 24 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar, or the combination of Takiar and Haba, and further in combination with Mathew.

Claims 24 and 27 depend from independent claims 20 and 25, respectively. Since claims 20 and 25 are clearly patentable as described above, the rejection of these claims also should be withdrawn. Further, as the examiner pointed out, Takiar does not disclose a bump formed on the second conductive portion in the second area (claim 24) and a first bump formed on the first area of the second conductive portion and the second bump formed on the third conductive pattern (claim 27). Regarding the bumps, the examiner states that Mathew teaches bumps. However, Mathew does not disclose where bumps should be formed. In other words, Mathew simply discloses general bump connection, whose bump are formed anywhere on a conductive contact point. Thus, Mathew does not disclose a bump formed on the second conductive portion in the second area (claim 24) and a first bump formed on the first area of the second conductive portion and the second bump formed on the third conductive pattern

(claim 27). Of course, Mathew does not disclose any characteristics claimed in claims 20 and 25.

since neither Takiar, Haba nor Mathew shows or suggests the characteristics described above, each of which is defined in claims 24 and 27, claims 24 and 27 are deemed to be clearly patentable, and the rejection of claims 24 and 27accordingly should be withdrawn.

In the action, claims 3-12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takiar, or the combination of Takiar and Haba, and further in combination with Mathew, or in alternative, further in combination with Mathew and Hill.

Claims 3-12 and claims 17 and 18 depend indirectly from independent claims 1 and 13, respectively. Since claims 20 and 25 are clearly patentable as described above, the rejection of these claims also should be withdrawn. As to the non-disclosure of bump connections, please refer to the above-described statement to claims 24 and 27. Further, the examiner asserts that although the combination of Takiar and Mathew does not disclose a longer and shorter sides of the rectangularly-shaped conductive relay pad, it would have bee an obvious matter of design choice to choose these particular dimensions. Applicant disagrees. When the longer side of the relay pad is parallel to a side of the semiconductor chip 3, large area on the first semiconductor chip can be secured for mounting the second semiconductor chip on the first chip. When the shorter side of the relay pad is parallel to a side of the semiconductor chip, it is possible to avoid contacting the first wire to the second wire while the area on the first semiconductor chip on which the second semiconductor chip is mounted, is restricted (Refer to the specification on page 7, line 16 – page 8, line 6).

Further, the examiner asserts that it would be an inherent property of the product obtained by routine experimentation that each of the longer and the shorter sides would be parallel to a side of the first semiconductor chip. Applicant disagrees. No cited reference disclose the relay pad having the longer side and the shorter side. Under this facts, Applicant respectfully requests to show any evidence to support the examiner's assertion.

Moreover, the examiner asserts that Hill teaches a longer and a shorter sides of a rectiangularly-shaped conductive bond pad 154a, each side parallel to a side of a first semiconductor chip 150. However, the bond pad 154a does **NOT** correspond to a relay pad of this invention because the bond pad 154a is connected to the bond pad 158a only. Thus, the bond pad 154a may correspond to a first terminal pad of the invention. Furthermore, the examiner asserts that it would have been obvious to combine the product of Hill with the product of Takiar because it would provide a pad. Applicant disagrees. As described above, since Takiar does not disclose the first and the second area of the relay pad, it would not have been obvious to combine the product of Hill with the product of Takiar. In addition, even if Hill teaches a pad, since Hill does not show any multi-chip package type semiconductor devices, Takiar and Hill cannot be combined because of the luck of motivation for combining them.

In view of the foregoing, the application is deemed to be in condition for allowance and such is earnestly solicited. Should any fee be needed, please charge it to our Account No. 50-0945 and notify us accordingly.

Attached hereto is a marked-up version of the changes made to the claims by

the current amendment. The attached page is captioned "**Version with markings to show changes made**".

Respectfully submitted

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 3-6, 8, 9, 17, 18 and 26 have been amended, as follows:

3 (amended). A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a first metal bump formed on the conductive relay pad in the first area and a second metal bump formed on the second terminal pad, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the first bonding wire is preformed at the first terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the first bonding wire is made at the first conductive pattern, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the second bonding wire is preformed at the second conductive pattern and a ~~the~~ second bond as an ~~the~~ ending connection of the second bonding wire is made at the first metal bump, and wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the third bonding wire is preformed at the conductive relay pad in the second area and a ~~the~~ second bond as an ~~the~~ ending connection of the third bonding wire is made at the second metal bump.

4 (amended). A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a metal bump formed on the conductive relay pad in the second area, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the first bonding wire is preformed at the first terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the first bonding wire is made at the first conductive pattern, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the second bonding wire is preformed at

the conductive relay pad in the first area and a ~~the~~ second bond as an ~~the~~ ending connection of the second bonding wire is made at the second conductive pattern, and wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the third bonding wire is preformed at the second terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the third bonding wire is made at the metal bump.

5 (amended). A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a ~~the~~ periphery of the first semiconductor chip, and a ~~the~~ longer side of the rectangularly-shaped conductive relay pad is parallel to a ~~the~~ side of the first semiconductor chip.

6 (amended). A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on a ~~the~~ periphery of the first semiconductor chip, and a ~~the~~ shorter side of the rectangularly-shaped conductive relay pad is parallel to a ~~the~~ side of the first semiconductor chip.

8 (amended). A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a ~~the~~ periphery of the first semiconductor chip, and a ~~the~~ longer side of the rectangularly-shaped conductive relay pad is parallel to a ~~the~~ side of the first semiconductor chip.

9 (amended). A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on a ~~the~~ periphery of the first semiconductor chip, and a ~~the~~ shorter side of the rectangularly-

shaped conductive relay pad is parallel to a ~~the~~ side of the first semiconductor chip.

17 (amended). A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a first metal bump formed on the conductive relay pad and a second metal bump formed on the second terminal pad, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the first bonding wire is preformed at the first terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the first bonding wire is made at the first conductive pattern, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the second bonding wire is preformed at the second conductive pattern and a ~~the~~ second bond as an ~~the~~ ending connection of the second bonding wire is made at the first metal bump, and wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the third bonding wire is preformed at the first metal bump and a ~~the~~ second bond as an ~~the~~ ending connection of the third bonding wire is made at the second metal bump.

18 (amended). A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a metal bump formed on the conductive relay pad, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the first bonding wire is preformed at the first terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the first bonding wire is made at the first conductive pattern, wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the second bonding wire is preformed at the conductive pattern and a ~~the~~ second bond as an ~~the~~ ending connection of the second bonding wire is made at the metal bump, and wherein a ~~the~~ first bond as a ~~the~~ beginning connection of the third bonding wire is preformed at the second terminal pad and a ~~the~~ second bond as an ~~the~~ ending connection of the third bonding wire is made at the metal bump.

26 (amended). A multi-chip package type semiconductor device, as claimed in claim 25, wherein the first area and the second areas are located along a ~~the~~ side of the first semiconductor chip.